

Scalable GaSb/InAs tunnel FETs with non-uniform body thickness

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(Dated: 19 July 2016)

GaSb/InAs heterojunction tunnel field-effect transistors are strong candidates in building future low-power integrated circuits, as they could provide both steep subthreshold swing and large ON-state current (I_{ON}). However, at short channel lengths they suffer from large tunneling leakage originating from the small band gap and small effective masses of the InAs channel. As proposed in this article, this problem can be significantly mitigated by reducing the channel thickness meanwhile retaining a thick source-channel tunnel junction, thus forming a design with a non-uniform body thickness. Because of the quantum confinement, the thin InAs channel offers a large band gap and large effective masses, reducing the ambipolar and source-to-drain tunneling leakage at OFF state. The thick GaSb/InAs tunnel junction, instead, offers a low tunnel barrier and small effective masses, allowing a large tunnel probability at ON state. In addition, the confinement induced band discontinuity enhances the tunnel electric field and creates a resonant state, further improving I_{ON} . Atomistic quantum transport simulations show that ballistic $I_{ON} = 284\text{A/m}$ is obtained at 15nm channel length, $I_{OFF} = 1 \times 10^{-3}\text{A/m}$, and $V_{DD} = 0.3\text{V}$. While with uniform body thickness, the largest achievable I_{ON} is only 25A/m . Simulations also indicate that this design is scalable to sub- 10nm channel length.

Tunnel field-effect transistor (TFET), a promising replacement of classical metal-oxide-semiconductor field-effect transistor (MOSFET) for future low-power integrated circuits, has been intensively studied over a decade. The advantages of TFET come from its steep subthreshold swing (SS) that overcomes the 60mV/dec limit of a conventional MOSFET, allowing substantial supply voltage (V_{DD}) scaling¹. However, because of low tunnel probability the steep SS usually occurs at very low current level^{2,3}. This leads to insufficient ON-state current (I_{ON}) and thus large switching delay (CV_{DD}/I_{ON}). Various approaches have been proposed to improve the low I_{ON} . In particular, GaSb/InAs heterojunction based TFETs can considerably boost I_{ON} due to their broken/staggered-gap band alignment^{4,5}.

However, as the channel length scales to sub- 20nm as projected by International Technology Roadmap for Semiconductors (ITRS) for the next technology nodes⁶, the GaSb/InAs n-type TFETs suffer from large ambipolar and source-to-drain tunneling leakage due to the small band gap and the small effective masses of the InAs channel. These leakage can be reduced by reducing the body thickness⁷, because the band gap and the effective masses of the InAs channel increase as the body thickness decreases. Meanwhile, the large band gap and large effective masses also reduce the tunneling probability across the tunnel junction. The resonant TFET with a reversed InAs/GaSb heterojunction can have a steep SS at short gate length⁷ but the I_{ON} is limited by the narrow resonant transmission peak⁸. The channel heterojunction design with a large band-gap AlInAsSb alloy as the channel material has also been proposed^{9,10} to mitigate the short-

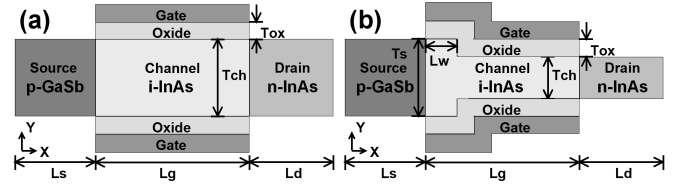


FIG. 1. GaSb/InAs n-type TFETs with conventional uniform (a) and proposed non-uniform (b) body thickness. The oxide and the gate in (b) are conformal to the channel so that the oxide thickness is equal to that of (a). Here, T_{ch}/T_{ox} is the channel/oxide thickness, ϵ_{ox} is the oxide dielectric constant, $L_s/L_g/L_d$ is the source/channel/drain length, and N_s/N_d is the source/drain doping density. The extra parameters in (b) are the source thickness T_s and the wide channel length L_w .

channel effects. However, a good-quality dielectric on top of AlInAsSb has not been experimentally demonstrated yet. Therefore, InP, a material with a high-quality dielectric already demonstrated, has been investigated as the alternative channel material¹¹. It is found that the lattice-mismatched InP channel imposes biaxial compressive strain on the GaSb/InAs tunnel junction, compromising the improvement.

In this study, we show that by reducing the InAs channel body thickness meanwhile retaining a relatively large body thickness at the source tunnel junction, the leakage can be significantly reduced without compromising the large source tunnel probability. The devices are simulated and optimized by solving Poisson equation and open-boundary Schrödinger equation¹² self-consistently within NEMO5 tool¹³. The Hamiltonian employed is in the atomistic $sp^3d^5s^*$ tight binding (TB) basis including spin-orbit coupling, with the room temperature TB parameters fitted to the band structures

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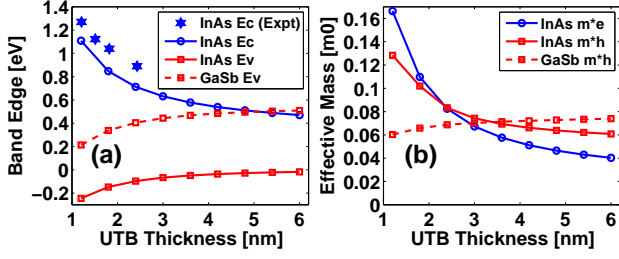


FIG. 2. (a) Conduction and valence band edges (Ec and Ev), (b) electron and hole effective masses (m^*e and m^*h), of the GaSb and InAs UTBs, as functions of the UTB thickness. The confinement is in the [001] orientation and the effective masses are in the [100] orientation.

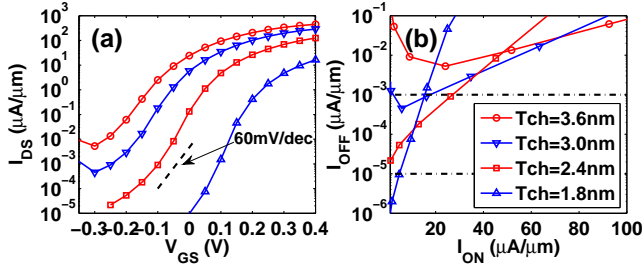


FIG. 3. (a) I_{DS} - V_{GS} characteristics ($V_{DS}=0.3V$) of the uniform device (Fig. 1 (a)) as a function of the body thickness Tch. Confinement/transport is in the [001]/[100] orientation. $L_g=15nm$, $T_{ox}=1.8nm$, $\epsilon_{ox}=9.0$, $N_s=-5 \times 10^{19}/cm^3$, and $N_d=+2 \times 10^{19}/cm^3$. (b) I_{ON} - I_{OFF} curves with $V_{DD} = 0.3V$.

as well as the wave functions of density functional theory calculations for better transferability^{14,15}. Due to the high semiconductor-to-oxide barrier height¹⁶, the oxide is treated as an impenetrable potential barrier and only modeled in the Poisson equation. Various scattering mechanisms, such as the electron-phonon scattering^{17,18} and the discrete dopant scattering¹⁹, are not included, which may lead to underestimated SS. Non-ideality effects, such as the interface trap assisted tunneling and the Shockley-Read-Hall generation-recombination processes²⁰, are not considered in this study.

First, we analyze the conventional GaSb/InAs UTB n-type TFETs with uniform body thickness, as illustrated in Fig. 1 (a). The band edges and the effective masses of the ultra-thin-body (UTB) structures for different body thicknesses are plotted in Fig. 2. As can be seen, the InAs UTB band gap (InAs Ec-InAs Ev) and the tunnel barrier height (InAs Ec-GaSb Ev) both increase as the UTB thickness becomes smaller. The InAs Ec calculated is in agreement with the experiment data²¹ with upto 0.2eV mismatch²². The effective masses (electron and hole) of the InAs UTB also increase significantly as the UTB thickness decreases. Therefore, the I-V characteristic of the device is a strong function of the UTB thickness. Indeed, as shown in Fig. 3 (a), a large body

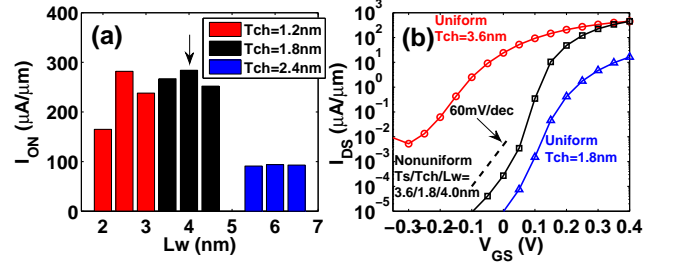


FIG. 4. (a) I_{ON} (at $V_{DD}=0.3V$ and $I_{OFF}=1 \times 10^{-3}A/m$) of the nonuniform design (Fig. 1 (b)) for different values of L_w and Tch, with fixed $T_s=3.6nm$. (b) Full I_{DS} - V_{GS} characteristics of the Ts/Tch/ $L_w=3.6nm/1.8nm/4.0nm$ case in (a), in comparison with the uniform 3.6nm and uniform 1.8nm cases. All other device parameters are the same as those in Fig. 3.

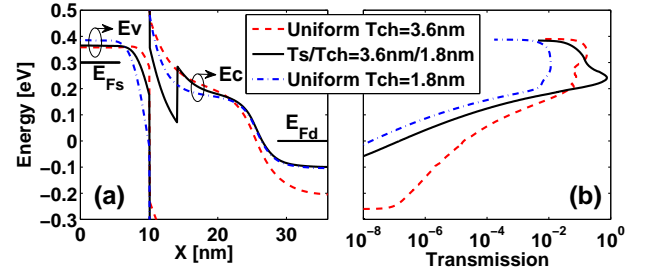


FIG. 5. Comparison of the band diagrams (a) and the transmission functions (b) of the three cases in Fig. 4 (b): uniform 3.6nm body thickness, uniform 1.8nm thickness, and non-uniform 3.6nm/1.8nm body thickness.

thickness (Tch=3.6nm or 3.0nm) leads to a large turn-on current, but also a large SS and a high I_{OFF} . A small body thickness (Tch=1.8nm) gives rise to a small SS and a low I_{OFF} , but a small turn-on current. With $I_{OFF} = 1 \times 10^{-3}A/m$ and $V_{DD} = 0.3V$, the optimal body thickness for $L_g=15nm$ is around 2.4nm, providing $I_{ON} = 25A/m$ (Fig. 3 (b)). This is too low for any practical logic application.

The proposed design that can overcome this dilemma is illustrated in Fig. 1 (b). Compared with Fig. 1 (a), this design has reduced body thickness *only* in part of the channel region (and in the drain). Three parameters need to be optimized, *i.e.*, T_s , Tch, and L_w . In this study, we fix T_s to be 3.6nm and then optimize Tch and L_w to maximize I_{ON} . As shown in Fig. 4 (a), there is an optimal L_w for each Tch and the optimal L_w is smaller for smaller Tch, which will be explained in a moment. A tradeoff of Tch is also clearly observed, since a large Tch does not have sufficiently large band gap and effective masses needed for the leakage suppression, while a small Tch would affect the ON-state transmission due to the large reflection at the waveguide discontinuity. With Tch=1.8nm and $L_w=4.0nm$, we obtain the largest I_{ON} (284A/m), which is more than an order of magnitude larger than that of the uniform case (25A/m). The full

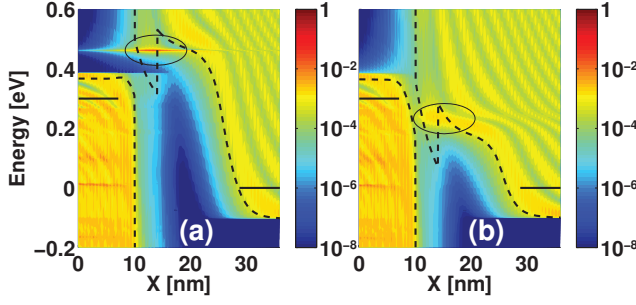


FIG. 6. LDOS (in logarithmic scale) of the optimized design in Fig. 4, at OFF state (a) and ON state (b). Band diagrams (dashed lines) and contact Fermi levels (solid lines) are superimposed. The quasi-bound states are highlighted (circles).

I_{DS} - V_{GS} curve is further displayed in Fig. 4 (b) along with two uniform thickness cases, showing that both steep SS and large turn-on current are simultaneously obtained in the nonuniform case.

The improvements can be better understood from the band diagrams and the transmissions plotted in Fig. 5, where the three cases in Fig. 4 (b) are compared. Above the channel E_c , the nonuniform 3.6/1.8nm case has larger transmission than the uniform 1.8nm case, giving rise to its larger turn-on current. This is due to its smaller tunneling barrier height and smaller effective masses at the tunnel junction. Its transmission over channel E_c is even larger than the uniform 3.6nm case, benefiting from its larger tunneling electric field and resonance-enhanced tunneling, both resulting from the confined band offset. Below the channel E_c , the nonuniform 3.6/1.8nm case has steeper transmission slope than the uniform 3.6nm case, implying steeper SS. This is partly due to the larger channel band gap and larger channel effective masses, partly due to the better electrostatics at the channel-drain junction, and partly due to the smaller drain Fermi degeneracy (the energy distance between the drain Fermi level and the drain E_c).

The local density of states (LDOS) is further depicted in Fig. 6. Similar to the channel heterojunction design⁹, the confined conduction band edges in the channel form a quantum well which creates a quasi-bound state. The energy level of this state needs to be aligned with the channel conduction band edge at the ON state so that it enhances the I_{ON} . At the OFF state, in order to reduce phonon-assisted tunneling leakage, the energy of this state has to be higher than the valence band edge at the source by at least the optical phonon energy²³ ($\hbar\omega_{op} \approx 30\text{meV}$ for bulk InAs and here it is 75meV higher). To satisfy these requirements, the parameter Lw needs to be adjusted for a given Tch, as shown in Fig. 4 (a). In fact, a smaller Tch leads to a larger confined band offset and thus the Lw needs to be reduced properly to shift the quasi-bound state upward.

Fig. 7 shows the sensitivities of the I-V curve to the geometry variations. We find that the I-V curve can toler-

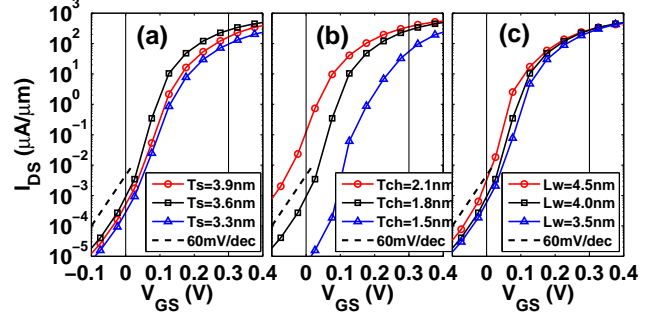


FIG. 7. Sensitivities of the I_{DS} - V_{GS} curve ($V_{DS}=0.3\text{V}$) to the variations of Ts (a), Tch (b), and Lw (d), for the optimized design in Fig. 4. The amount of Ts and Tch variations is one monolayer (about $\pm 0.3\text{nm}$) and the Lw variation is $\pm 0.5\text{nm}$.

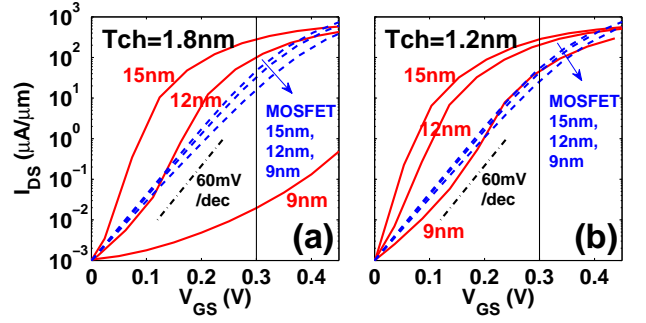


FIG. 8. I_{DS} - V_{GS} characteristics ($V_{DS}=0.3\text{V}$) of the proposed TFETs, in comparison with Si MOSFETs, for three channel lengths ($L_g=15\text{nm}$, 12nm , and 9nm). (a) Ts/Tch/Lw=3.6/1.8/4.0nm for TFETs and Tch=1.8nm for MOSFETs, and (b) Ts/Tch/Lw=3.6/1.2/2.5nm for TFETs and Tch=1.2nm for MOSFETs.

ate certain amount of Ts and Lw variations. It is however very sensitive to the channel thickness (Tch) variations resulting in unacceptable I_{OFF} or I_{ON} level. This suggests that precise fabrication control of Tch (at atomic level) is necessary.

ITRS 2020 and 2023 technology nodes require channel length L_g to be scaled to about 12nm and 9nm⁶. At such short channel lengths, the source-to-drain tunneling leakage becomes more prominent. As compared in Fig. 8 (a), when L_g is reduced from 15nm to 12nm, the I_{ON} of TFET drops from 284A/m to 106A/m, while the I_{ON} of Si MOSFET only drops from 49A/m to 41A/m. When L_g is further scaled to 9nm, the TFET cannot provide a decent ON/OFF ratio and does not possess an advantage over Si MOSFET. To improve the scalability, the channel thickness (Tch) can be reduced from 1.8nm to 1.2nm to enlarge the channel band gap and channel effective masses. As seen in Fig. 8 (b), the SS of TFET degrades less, with $I_{ON}=209\text{A/m}$ (50A/m) obtained at $L_g=12\text{nm}$ (9nm), which is still considerably larger than $I_{ON}=47\text{A/m}$ (31A/m) of Si MOSFET.

In summary, a novel transistor design with a nonuniform body thickness is proposed to improve the scala-

bility of GaSb/InAs n-type TFETs. At 15nm channel length, it achieves ballistic I_{ON} that is over $10\times$ greater than that is achievable with uniform body thickness. Moreover, it enables the channel to be scaled towards sub-10nm lengths. This design can also be employed to improve InAs/GaSb p-type TFETs.

This work uses nanoHUB.org computational resources operated by the Network for Computational Nanotechnology funded by the U.S. National Science Foundation under Grant EEC-0228390, Grant EEC-1227110, Grant EEC-0634750, Grant OCI-0438246, Grant OCI-0832623, and Grant OCI-0721680. This material is based upon work supported by the National Science Foundation under Grant 1509394. NEMO5 developments were critically supported by an NSF Peta-Apps award OCI-0749140 and by Intel Corp.

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²²The experimental data is shifted by 0.15eV to account for the valence band offset (VBO) between bulk InAs and confined AlSb (with 5nm thickness), assuming the VBO between bulk InAs and bulk AlSb is 0.18eV²⁴ and the confined heavy hole energy of 5nm thickness AlSb UTB is 0.03eV in our TB calculation. Note that the experiment data were obtained at low temperature.

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